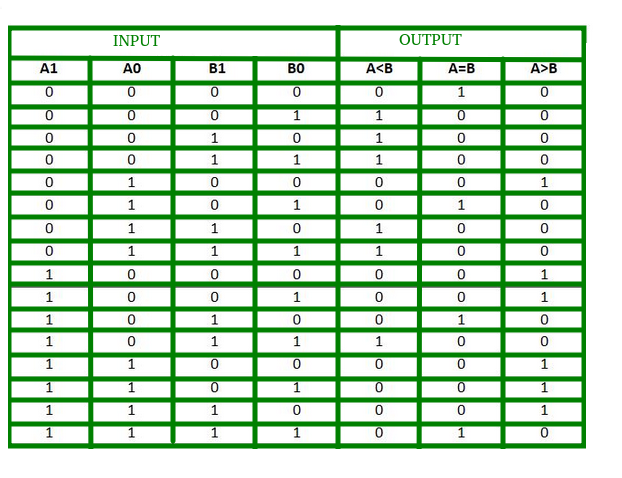
**EXPERIMENT – 10**

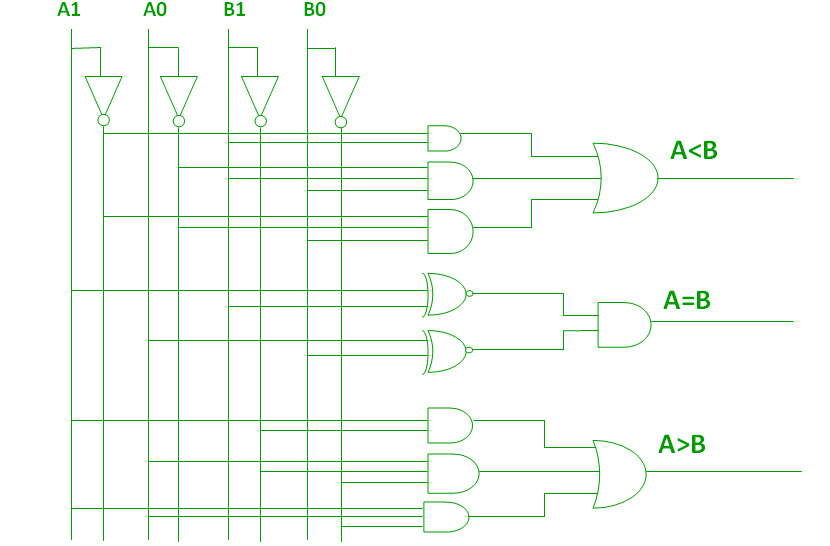
**AIM** - WRITE A VHDL POROGRAM FOR 2 BIT COMPARATOR AND SIMULTE IT

USING MODELSIM.

**THEORY** - A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

TRUTH TABLE



DIAGRAM

**VHDL CODE:**

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.std\_logic\_arith.all;

ENTITY COMPARATOR\_2BIT IS

Port( A,B: in std\_logic\_vector(1 downto 0);

A\_less\_B: out std\_logic;

A\_equal\_B: out std\_logic;

A\_greater\_B: out std\_logic

);

END ENTITY COMPARATOR\_2BIT;

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ARCHITECTURE COMPARATOR\_2BIT\_STRUCT OF COMPARATOR\_2BIT IS

component AND\_GATE

port(A,B:in std\_logic;Z: out std\_logic);

end component;

component XNOR\_GATE

port(A,B:in std\_logic;Z: out std\_logic);

end component;

component OR\_GATE

port(A,B:in std\_logic;Z: out std\_logic);

end component;

component NOT\_GATE

port(A:in std\_logic;Z: out std\_logic);

end component;

SIGNAL TEMP:STD\_LOGIC\_VECTOR(17 DOWNTO 0);

BEGIN

N1 : NOT\_GATE port map (A(0),TEMP(0));

N2 : NOT\_GATE port map (A(1),TEMP(1));

N3 : NOT\_GATE port map (B(0),TEMP(2));

N4 : NOT\_GATE port map (B(1),TEMP(3));

XN1: XNOR\_GATE port map (A(0),B(0),TEMP(4));

XN2: XNOR\_GATE port map (A(1),B(1),TEMP(5));

A1 : AND\_GATE port map (TEMP(4),TEMP(5),A\_equal\_B);

A2 : AND\_GATE port map (A(1),TEMP(3),TEMP(6)); --TEMP 6

A3 : AND\_GATE port map (TEMP(2),TEMP(3),TEMP(7));

A4 : AND\_GATE port map (A(0),TEMP(7),TEMP(8)); --TEMP 8

A5 : AND\_GATE port map (A(1),A(0),TEMP(9));

A6 : AND\_GATE port map (TEMP(2),TEMP(9),TEMP(10)); --TEMP 10

O1 : OR\_GATE port map (TEMP(6),TEMP(8),TEMP(11));

O2 : OR\_GATE port map (TEMP(10),TEMP(11), A\_greater\_B);

A7 : AND\_GATE port map (TEMP(1),B(1),TEMP(12)); --TEMP 12

A8 : AND\_GATE port map (TEMP(0),B(1),TEMP(13));

A9 : AND\_GATE port map (B(0),TEMP(13),TEMP(14)); --TEMP 14

A10: AND\_GATE port map (TEMP(0),TEMP(1),TEMP(15));

A11: AND\_GATE port map (B(0),TEMP(15),TEMP(16)); --TEMP 16

O3 : OR\_GATE port map (TEMP(12),TEMP(14),TEMP(17));

O4 : OR\_GATE port map (TEMP(16),TEMP(17), A\_less\_B);

END ARCHITECTURE COMPARATOR\_2BIT\_STRUCT;

ARCHITECTURE COMPARATOR\_2BIT\_DATAFLOW OF COMPARATOR\_2BIT IS

BEGIN

A\_greater\_B <=( (A(1) AND (NOT B(1))) OR (A(0) AND (NOT B(1)) AND (NOT B(0))) OR (A(1) AND A(0) AND (NOT B(0))) );

A\_equal\_B <=( (A(0) XNOR B(0)) AND (A(1) XNOR B(1)) );

A\_less\_B <=( ((NOT A(1) AND B(1))) OR ((NOT A(0)) AND B(1) AND B(0)) OR ((NOT A(1)) AND (NOT A(0)) AND B(0)) );

END ARCHITECTURE COMPARATOR\_2BIT\_DATAFLOW;

ARCHITECTURE COMPARATOR\_2BIT\_BEHAV OF COMPARATOR\_2BIT IS

BEGIN

process(A,B)

begin

if(A<B) then

A\_less\_B <='1';

A\_equal\_B <='0';

A\_greater\_B <='0';

elsif(A>B) then

A\_less\_B <='0';

A\_equal\_B <='0';

A\_greater\_B <='1';

else

A\_less\_B <='0';

A\_equal\_B <='1';

A\_greater\_B <='0';

end if;

end process;

END ARCHITECTURE COMPARATOR\_2BIT\_BEHAV;

**RESULT:**

